

We Claim:

1 1. An integrated dynamic memory, comprising:
2 a plurality of memory cells, the memory cells being combined to form
3 individual independently addressable units; and
4 a control circuit for controlling a refresh mode for the memory cells, the
5 memory cells having their memory cell content refreshed during the refresh mode,
6 the control circuit being designed such that one or more units of memory cells
7 can be subject to the refresh mode in parallel in a refresh cycle, the control circuit setting
8 a number of memory cell units which are to be refreshed in parallel in a refresh cycle
9 based on a temperature reference value.

1 2. The integrated dynamic memory as claimed in claim 1, wherein the control
2 circuit has a changeover mechanism such that, if a first limit temperature reference value
3 is exceeded, a selected unit of memory cells and at least one further unit of memory cells
4 are subject to the refresh mode in parallel in the refresh cycle.

1 3. The integrated dynamic memory as claimed in claim 1, wherein the memory
2 is organized into word lines and bit lines, the memory cells being arranged at crossover
3 points between the word lines, the memory cells bit lines and being connected to a
4 respective word line and bit line, the memory cells in units of a whole word line subject
5 to a refresh mode in a refresh cycle, and the control circuit sets a number of word lines
6 which are to be refreshed in parallel in a refresh cycle based on the temperature reference
7 value.

1 4. The integrated dynamic memory as claimed in claim 3,
2 wherein the memory has a number of n word lines, the control circuit has a changeover
3 mechanism such that, if a first limit temperature reference value is exceeded, a selected
4 word line and a word line shifted by the number of $n/2$ word lines are select and are
5 subjected to a refresh mode in parallel in a refresh cycle.

1 5. The integrated dynamic memory as claimed in claim 4, wherein the control
2 circuit has a changeover mechanism such that, if a second limit temperature reference
3 value increased by a temperature interval is exceeded, not only the selected word line and
4 a respective word line shifted by the number of $n/4$, $n/2$, and $3n/4$ word lines are
5 subjected to a refresh mode in parallel in a refresh cycle.

1 6. The integrated dynamic memory as claimed in claim 5, wherein the
2 temperature interval has been set in the control circuit to a half-value temperature which
3 identifies a temperature interval within which the data retention time of the memory cells
4 is halved.

1 7. The integrated dynamic memory as claimed in claim 1, wherein the control
2 circuit has a counter circuit for addressing memory cell units which are to be refreshed,
3 which receives a refresh command and a multiplexer circuit, and the multiplexer being
4 actuated by the counter circuit for selecting the units ($WL0$ to $WLn-1$) of memory cells
5 for a refresh mode, where the multiplexer circuit receives a control signal (R) which
6 transmits the temperature reference value.

1 8. The integrated dynamic memory as claimed in claim 1, wherein
2 the temperature reference value is generated by a temperature sensor circuit which is
3 arranged on the memory.

1 9. The integrated dynamic memory as claimed in claim 1, wherein
2 the control circuit is designed such that a plurality of units of memory cells can be subject
3 to a refresh mode in parallel in a refresh cycle, the refresh mode being staggered over
4 time within a refresh interval.